1 **WHAT IS CLAIMED IS:**

2   1. A memory interlace-checking method to detect weakened memory, which

3 comprises:

4   a main step, which has at least one main address accessing datum and

5   commands to perform actions on each memory address;

6   a data checking step, which includes an address accessing datum

7   containing data checking commands that check data in part of the

8   addresses complementary to the main address accessing datum.

9   2. The method of claim 1, wherein the main step performs command actions

10 on interlacing memory rows.

11   3. The method of claim 1, wherein the main step performs command actions

12 on interlacing memory columns.

13   4. A memory interlace-checking method to detect weakened memory, which

14 is implemented in a test program with a command action, the test program

15 comprising:

16   at least a portion of main address accessing data; and

17   at least a portion of secondary address accessing data, which is at least

18   partially complementary to the portion of main address accessing data.

19   5. The method of claim 4, wherein the main address accessing data contains

20 the command actions.

21   6. The method of claim 4, wherein the secondary address accessing data

22 contains a checking action.

23   7. A memory interlace-checking method to detect weakened memory, which

24 comprises:

8

an access step, which contains at least a main address accessing datum
to perform command actions on the odd (even) address units of
memory;

a checking step, which contains at least an address accessing datum and
check data stored in the even (odd) address units of memory that have
yet to be accessed in the access step.

8. The method of claim 7, wherein the address unit is a row.

9. The method of claim 7, wherein the address unit is a column.

10. The method of claim 7, wherein the checking step contains a checking
command.